

Docket No.: 49657-962

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Re Application of

Yoshio FUDEYASU

Serial No.: 09/769,417

Group Art Unit: 2187

Filed: January 26, 2001

Examiner: Mehdi NAMAZI

For: SEMICONDUCTOR MEMORY DEVICE AND MEMORY SYSTEM USING THE SAME

THE COMMISSIONER FOR PATENTS AND TRADEMARKS  
Washington, DC 20231

Dear Sir:

Transmitted herewith is an Amendment in the above identified application.

☒  
☐  
☐

No additional fee is required.

Applicant is entitled to small entity status under 37 CFR 1.27

Also attached:

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Technology Center 2100

The fee has been calculated as shown below:

	NO. OF CLAIMS	HIGHEST PREVIOUSLY PAID FOR	EXTRA CLAIMS	RATE	FEE
Total Claims	15	20	0	\$18.00 =	\$0.00
Independent Claims	3	3	0	\$84.00 =	\$0.00
Multiple claims newly presented					\$0.00
For for Information Disclosure Statement					\$180.00
Total of Above Calculations					\$0.00
					\$180.00

☒ Please charge my Deposit Account No. 500417 in the amount of \$180.00. An additional copy of this transmittal sheet is submitted herewith.

☒ The Commissioner is hereby authorized to charge payment of any fees associated with this communication or credit any overpayment, to Deposit Account No. 500417, including any filing fees under 37 CFR 1.16 for presentation of extra claims and any patent application processing fees under 37 CFR 1.17.

Respectfully submitted,

MCDERMOTT, WILL & EMERY

*David M. Tennant*  
David M. Tennant

Registration No. 48,362

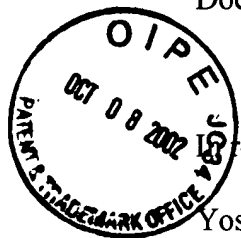
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5/A  
CO-16-AL  
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For: SEMICONDUCTOR MEMORY DEVICE AND MEMORY SYSTEM USING  
THE SAME

AMENDMENT

Commissioner for Patents  
Washington, DC 20231

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Sir:

In response to the Office Action dated July 8, 2002, please amend the above-identified application as follows:

IN THE CLAIMS:

Please ~~cancel~~ claims 1 and 2 in their entirety without prejudice or disclaimer of the subject matter thereof.

Claims 3, 4 and 15 now read as follows:

- A1 Sub 131
3. (Amended) A semiconductor memory device comprising:  
a plurality of input terminals for receiving write data, a control signal and an address signal; and  
at least one output terminal, different in number from the input terminal(s) for receiving the write data, for outputting read data, wherein the input terminals are coupled